

## LINEAR FEEDBACK SHIFT REGISTER RESEEDING

### Abstract

5 An apparatus has an integrated circuit that includes a seed register, a linear  
feedback shift register to load a test vector into a number of scan chains, and a  
signature register to receive a test response from the scan chains. The seed register,  
the linear feedback shift register, and the signature register each have the same  
register length. The linear feedback shift register and the signature register have the  
same shift frequency that is greater than a frequency at which a seed vector is  
10 loaded into the seed register. The linear feedback shift register is adapted to be  
selectively provided with bits to control a degree to which its vector is dependent on  
previous vectors. The scan chains may be configured as a single group providing a  
test response to a single input signature register or a set of groups providing a test  
response to a multiple input signature register.

15

"Express Mail" mailing label number: EV332567793US

Date of Deposit: September 19, 2003

This paper or fee is being deposited on the date indicated above with  
the United States Postal Service pursuant to 37 CFR 1.10, and is  
addressed to the Commissioner for Patents, Mail Stop Patent  
Application, P.O. Box 1450, Alexandria, VA 22313-1450.